RESEARCH ARTICLE OPEN ACCESS

Modified Shuffled Iterative Encoding For Binary Ldpc Codes

S. Renugavathi, R. Kalpana, R.P.Rubajini, R.Rajalakshmi
(M.E),
M.E, Asst. Professor
M.E, Asst. Professor
M.E, Asst. Professor
VeltechMultitechDr.RangarajanDr.SakunthalaEngg College, Chennai.

Abstract
Flexible and reconfigurable architectures have gained wide popularity in the field of communication. Particularly, reconfigurable architectures help in achieving switching among various coding modes and also inoperability. This work concentrates on the design of a reconfigurable architecture for both turbo and LDPC codes decoding. The major contributions of this work are: i) tackling the reconfiguration issue introducing a formal and systematic treatment that, to the best of our knowledge, was not previously addressed and ii) proposing a reconfigurable LDPC decoder architecture and showing that wide flexibility can be achieved with a small complexity overhead. Obtained results show that dynamic switching between most of considered communication standards is possible without pausing the decoding activity.

I. INTRODUCTION

LDPC codes were invented by Robert Gallager in his PhD thesis. Soon after their invention, they were largely forgotten, and reinvented several times for the next 30 years. Their comeback is one of the most intriguing aspects of their history, since two different communities reinvented codes similar to Gallager's LDPC codes at roughly the same time, but for entirely different reasons. LDPC codes are defined as the linear codes obtained from a sparse bipartite graph. Suppose that G is a graph with n left nodes (called message nodes) and r right nodes (called check nodes). A linear code of block length 'n' is obtained from the graph and dimension at least n x r in the following way: The n coordinates of the codewords are associated with the n message nodes. The codewords are those vectors (c_1; : : : ; c_n) such that for all check nodes the sum of the neighboring positions among the message nodes is zero.

Several different algorithms exist to construct desired LDPC codes. Gallagerintroduced one such LDPC code. Furthermore MacKay proposed one to semi-randomly generate sparse parity check matrices. This is quite interesting since it indicates that constructing good performing LDPC codes is not a hard problem. In fact, completely randomly chosen codes are good with a high probability. The problem that will arise, is that the encoding complexity of such codes is usually rather high.

Depending on the approach to exploit parallelism in the decoding algorithm of the code, LDPC decoders are divided into two main categories: full-parallel and partial-parallel decoders. In full-parallel decoders, every processing node is implemented in hardware, and these nodes are connected through global wires based on the parity check matrix. In partial-parallel architectures, a subset of check nodes and variable nodes of the parity check matrix is implemented in hardware.

While proposing LDPC codes in his PhD thesis, Robert Gallager also provided a decoding algorithm, which is called probabilistic decoding. This decoding algorithm is typically near optimal. For different application purposes, different decoding algorithms have been developed after Robert Gallager's work, including belief propagation algorithm, sum-product algorithm, min-sum algorithm and so on. These iterative algorithms are also called message passing algorithms, due to the fact that "messages" are computed and passed between variable nodes and check nodes during their decoding process.

II. II PROPOSED MODEL

In the proposed method sparse matrix will be reduced and in such a way that all the process will be done in parallel. Input data which need to be send will be divided into parts and will be given to sparse matrix so every part will be processed in parallel so total system complexity will be decreased.

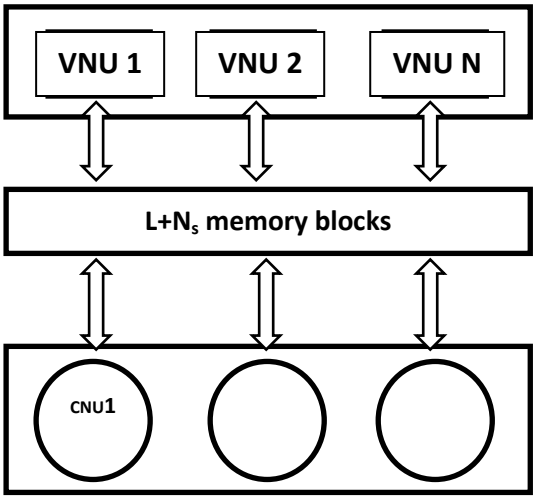
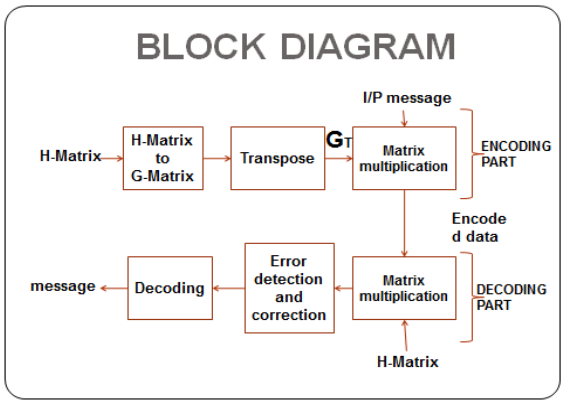


FIG.1 DIVIDED SPARSE MATRIX BASED LDPC

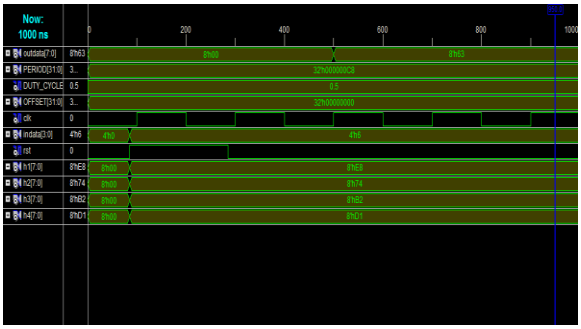
The main blocks of LDPC are variable node unit (VNU), check node unit(CNU) and sparse matrix. Sparse matrix contains the connections between VNUs and CNUs.



III. SHUFFLED ITERATIVE ENCODING

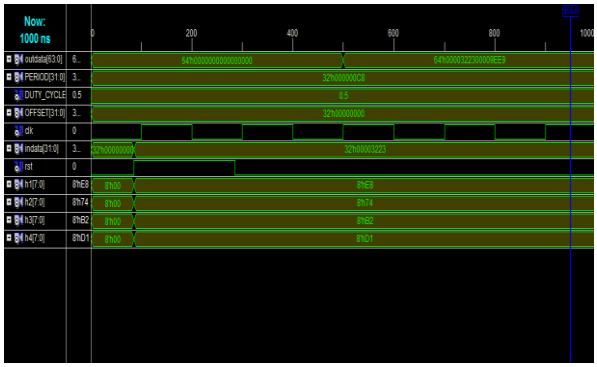
The aim of the project is to perform encoding and decoding over non-binary LDPC codes of 4-bit and 32-bit signals. Out of these, the encoding part has been performed in this phase. That is, the non-binary LDPC codes have been encoded. This is carried out by generating a sparse matrix. The encoding has been applied to signals at various stages and the simulation results so obtained, are shown in the following figures.

Simulation result for 4 bit LDPC



The above figure shows the simulation output of a 4-bit LDPC. In the proposed system, this simulation is carried out for non-binary LDPC codes. The inputs are given at various clock cycles and the encoded outputs of various stages are determined.

Simulation result for 32 bit LDPC



The above figure shows the simulated result of a 32-bit LDPC. The LDPC encoding for non-binary LDPC codes are carried out in this module and the encoded outputs for 32-bit signals are determined.

IV. CONCLUSION

In this brief, we proposed an iterative shuffled encoding of binary LDPC codes. In the shuffled iterative algorithm, the code length is divided into a number of groups. The updating of messages is done in parallel. However, the processing is carried out one by one.

The future enhancement of this proposed system is to perform decoding over these binary LDPC codes. Thus, a complete modified shuffled iterative decoding is done for the binary LDPC codes.

References

[1] Jun Lin and Zhiyuan Yan," Efficient Shuffled Decoder Architecture for Nonbinary Quasi-Cyclic LDPC Codes" *IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst.*, vol. 16, no. 5, pp. 565–578, Sep. 2013.

[2] Y. Dai, Z. Yan, and N. Chen, "Optimal overlapped message passing decoding of

quasi-cyclic LDPC codes," *IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst.*, vol. 16, no. 5, pp. 565–578, May 2008.

[3] Z. Zhang, L. Dolecek, B. Nikolic, V. Anantharam, and M.Wainwright, "Investigation of error floors of structured low-density parity-check codes by hardware emulation," in *Proc. IEEE Global Telecommun.Conf.*, Dec. 2006, pp. 1–6.

[4] Z. Li, L. Chen, L. Zeng, S. Lin, and W. Fong, "Efficient encoding of quasi-cyclic low-density parity-check codes," *IEEE Trans. Commun.*, vol. 53, no. 11, p. 1973, Nov. 2005.

[5] L. Chen, J. Xu, I. Djurdjevic, and S. Lin, "Near-Shannon-limit quasicyclic low-density parity-check codes," *IEEE Trans. Commun.*, vol. 52, no. 7, pp. 1038–1042, Jul. 2004.

[6] D. MacKay, "Good error-correcting codes based on very sparse matrices," *IEEE Trans. Inf. Theory*, vol. 45, no. 2, pp. 399–431, Mar. 1999.

[7] M. Fossorier, M. Mihaljevic, and H. Imai, "Reduced complexity iterative decoding of low-density parity check codes based on belief propagation," *IEEE Trans. Commun.*, vol. 47, no. 5, pp. 673–680, May 1999.

[8] D. MacKay, "Good error-correcting codes based on very sparse matrices," *IEEE Trans. Inf. Theory*, vol. 45, no. 2, pp. 399–431, Mar. 1999.

[9] M. Fossorier, M. Mihaljevic, and H. Imai, "Reduced complexity iterative decoding of low-density parity check codes based on belief propagation," *IEEE Trans. Commun.*, vol. 47, no. 5, pp. 673–680, May 1999.